Hall Ticket Number:

Code No. : 14215 N/O

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (CSE: CBCS) IV-Semester Main & Backlog Examinations, May-2019

Computer Architecture

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q.No.	Stem of the question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	Write the two register transfer statements for the following operations. If(M=1) then (R2←R1) else if (N=1) then (R4←R3)	2	3	1	1,2
2.	A digital computer has a common bus system for 16 registers of 32 bits each. What size of multiplexers is needed if a bus is to be constructed using multiplexers?	2	3	1	1,2
3.	Differentiate between hard-wired and micro programmed control unit.	2	2	2	1
4.	Draw the control flow chart for the memory reference instruction LDA.	2	2	2	1
5.	Determine effective address if relative address mode is used on instruction stored at location 300 with the address value in the instruction as 100.	2	3	3	1,2
6.	What are the advantages of Pipelining?	2	2	3	1
7.	When do you prefer software polling to interrupt driven I/O?	2	2	4	1,2
8.	How many characters are transferred for a baud rate of 600?	2	2	4	1,2
9.	How many 128 x 8 memory chips are needed to provide a memory capacity of 4086 x 16?	2	3	5	1,2
10.	What is the importance of cache memory?	2	2	5	1
	Part-B (5 × 8 = 40 Marks)				
11.a)	Design a bus system for 8 registers with 8 bits each using Multiplexers.	4	2	1	1,2,3
b)	A computer uses a memory unit with 512K words of 16 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. i) How many bits are there in the operation code, the register code part and the address part? ii) How many bits are there in the data and address inputs of the memory?	4	3	1	1,2,3
12.a)	Differentiate between RISC and CISC architectures.	4	2	2	1
b)	The content of PC in the basic computer is 3AF (all numbers are in hexadecimal). The content of AC is 7EC3. The content of memory at address 3AF is 932E. The content of memory at address 32E is 09AC. The content of memory at address 9AC is 8B9F. i) What is the instruction that will be fetched and executed next? ii) Determine the effective address if indirect address mode is applied.	4	3	2	1,2,3

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13.a)	Explain instruction pipeline conflicts and their remedies.	4	2	3	1,2
b)	A computer uses a memory of 65,536 words with eight bits in each word. It has the following registers: PC, AR, TR(16 bits each), and AC, DR, IR(eight bits each). A memory-reference instruction consists of three words: an 8-bit operation code (one word) and a 16-bit address (in the next two words). All operands are eight bits. There is no indirect bit. Draw a block diagram of the computer showing the memory and registers.	4	3	3	1,2,3
14.a)	What is an I/O processor? Explain with a neat Diagram.	4	2	4	1,2,3
b)	Design parallel priority interrupt hardware for a system with 12 interrupt sources.	4	3	4	1,2,3
15.a)	What factors affect the performance of CPU? How is the performance of CPU evaluated?	4	2	5	1,2
b)	A computer has a single cache (off-chip) with a 2 ns hit time and a 98% hit rate. Main memory has a 40 ns access time. What is the computer's effective access time? If we add an on-chip cache with a 0.5 ns hit time and a 94% hit rate, what is the computer's effective access time? How much speedup does the on-chip cache give the computer?	4	3	5	1,2,3
16.a)	What type of instructions to be included to make instruction set complete? Explain basic organization of control unit in a computer.	4	2	2	1,2,3
b)	Design a 4-bit decrementer circuit using four full-adder circuits.	4	2	1	1,2,3
17.	Answer any ***two*** of the following:				
a)	Explain Booth's multiplication algorithm with an example.	4	2	3	1,2,3
b)	Design a priority interrupt hardware using daisy chain priority mechanism for the devices with priority D3, D5, D1, D4 and D2.	4	3	4	1,2,3
c)	Explain memory hierarchy in a computer.	4	2	5	1

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	60
2	Knowledge on application and analysis (Level-3 & 4)	40
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	